GNQ5L0C31

QSFP28,100Gb/s,1294 -1310nm,SMF,40KM,DDM,LC

Features

- 4 channels full-duplex transceiver module
- Supports data rate up to 103.1Gb/s
- Supports QSFP28 4WDM 40km MSA
- 4 DFB-based LAN-WDM cooling transmitter
- 4 channels APD ROSA
- Internal CDR circuits on both receiver and transmitter channels
- Low power consumption <3.8W
- Hot pluggable QSFP form factor
- Up to 30km reach for G.652 SMF without FEC
- Up to 40km reach for G.652 SMF with FEC
- Duplex LC receptacle
- Built-in digital diagnostic function
- Operating case temperature 0° C to +70° C
- 3.3V power supply voltage
- RoHS 6 compliant (lead free)

Application

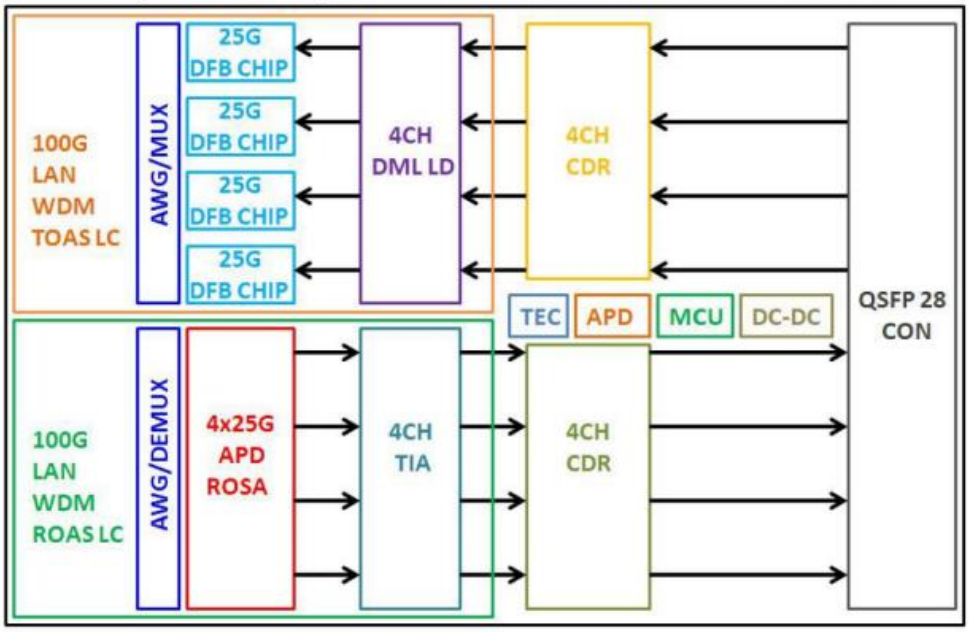
- IEEE 802.3ba 100GBASE-ER4 links
- Client-side 100G interconnections

Description

This product is a 100Gb/s transceiver module designed for optical communication applications compliant to QSFP28 4WDM-40 MSA standard. The module converts 4 input channels of 25Gb/s electrical data to 4 channels of LAN WDM optical signals and then multiplexes them into a single channel for 100Gb/s optical transmission. Reversely on the receiver side, the module de-multiplexes a 100Gb/s optical input into 4 channels of LAN WDM optical signals and then converts them to 4 output channels of electrical data. The central wavelengths of the 4 LAN WDM channels are 1295.56, 1300.05, 1304.58 and 1309.14 nm as members of the LAN WDM wavelength grid defined in IEEE 802.3ba. The high performance cooled LAN WDM DFB transmitters and high sensitivity APD receivers provide superior performance for 100Gigabit Ethernet applications up to 30km links without FEC and up to 40km links with FEC interconnections.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP MSA. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

QSFP28 ER4/4WDM 40km CIRCUIT STRUCTURE



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Supply Voltage	Vcc	-0.3	3.6	V	
Input Voltage	Vin	-0.3	Vcc+0.3	V	
Storage Temperature	Tst	-20	85	°C	
Case Operating Temperature	Top	0	70	°C	
Humidity(non-condensing)	Rh	5	85	%	
Damage Threshold,each Lane	TH	5.5		dB	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Supply Voltage	Vcc	3.13	3.3	3.47	V	
Case Operating Temperature	Tca	0		70	V	
Data Rate Per Lan	fd		25.78125		Gbps	
Humidity	Rh	5		85	%	
Power Dissipation	P			3.8	W	
Link Distance with G.652(with FEC)	D	0.02		40	km	

Electrical Specificationgs

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Power Consumption	P			3.8	W	
Supply Current	Icc			1.06	A	
Transceiver Power-on Initialization				2000	ms	
Transmitter (each Lane)						
Single-ended Input Voltage		-0.3	-	4.0	V	
AC Common Mode Input Voltage Tolerance		15	-		mV	
Differential Input Voltage		50	-		mVpp	
Differential Input Voltage Swing	V_{IN}		-	900	mVpp	
Differential Input Impedance	Zin	90	100	110	Ohm	
Receiver (each Lane)						
Single-ended Output Voltage		-0.3	-	4.0	V	
AC Common Mode Output		-	-	7.5	mV	
Differential Output Voltage Swing	V_{OUT}	300	-	850	mVpp	
Differential Output Impedance	Z_{OUT}	90	100	110	Ohm	

Note:
Power-on Initialization Time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the module is fully functional.

Optical Characteristics

Table 3 - Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Lane Wavelength	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.19	nm	
Transmitter						
SMSR	SMSR	30			dB	
Total Average Launch	PT			12.5	dB	
Average Launch Power, each Lane	PAVG	-2.5		6.5	dB	
OMA, each Lane	POMA	0.5		6.5	dB	1
Difference in Launch	Ptx,diff			3	dB	
Launch Power in OMA		-0.5			dB	
TDP, each Lane	TDP			3.0	dB	
Extinction Ratio	ER	4.5			dB	
$RIN_{20}OMA$	RIN			-130	dB/	
Optical Return Loss	TOL			20	H dB	

Transmitter Reflectance	RT			-12	dB	
Eye Mask coordinates: X1, X2,		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				2
Average Launch Power OFF	Poff			-30	dB	
Receiver						
Damage Threshold, each Lane	TH_d	-6			dB	3
Average Receive Power, each		-20.5		-7	dB	
Receiver Sensitivity (OMA), each Lane（BER = $5x10^{-5}$）	SEN1			-16.5	dBm	
Receiver Sensitivity (OMA), each Lane（BER = $1x10^{-12}$）	SEN1			-15	dBm	
StressedReceiver Sensitivity (OMA), each Lane（BER = $x10^{-5}$）				-16	dBm	4
Difference in Receive Power between any Two Lanes (OMA)	Prx,diff			3.6	dB	
LOS Assert	LOSA		-26		dBm	
LOS Deassert	LOSD		-24		dBm	
LOS Hysteresis	LOSH	0.5		31	dB	
Receiver Electrical 3 dB upper Cutoff Frequency, each Lane	Fc				GHz	
Conditions of Stress Receiver Sensitivity Test(Note5)						
Vertical Eye Closure Penalty, each Lane			2.5		dB	5
Stressed Eye J2 Jitter, each Lane			0.33		UI	
Stressed Eye J9 Jitter, each Lane			0.48		UI	

Note:

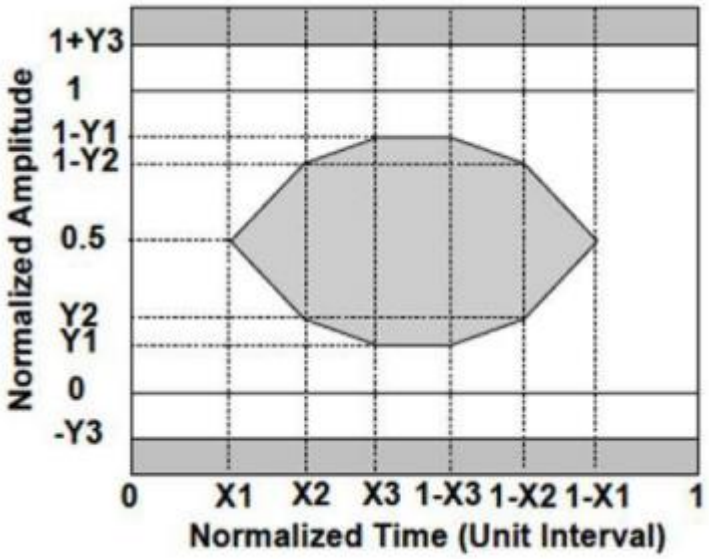
1. Even if the TDP < 1 dB, the OMA min must exceed the minimum value specified here.

2. See Figure 4 below.

3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

4. Measured with conformance test signal at receiver input for BER = $5x10^{-5}$.

5. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.



Pin Descriptions

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Module Ground	1
2	CML-I	Tx2-	Transmitter inverted data input	
3	CML-I	Tx2+	Transmitter non-inverted data input	
4		GND	Module Ground	1
5	CML-I	Tx4-	Transmitter inverted data input	
6	CML-I	Tx4+	Transmitter non-inverted data input	
7		GND	Module Ground	1
8	LVTTL-I	MODSEI	Module Select	2
9	LVTTL-I	ResetL	Module Reset	2
10		VCCRx	+3.3v Receiver Power Supply	
11	LVCMOS-I	SCL	2-wire Serial interface clock	2
12	LVCMOS-	SDA	2-wire Serial interface data	2
13		GND	Module Ground	1
14	CML-O	RX3+	Receiver non-inverted data output	
15	CML-O	RX3-	Receiver inverted data output	
16		GND	Module Ground	1
17	CML-O	RX1+	Receiver non-inverted data output	
18	CML-O	RX1-	Receiver inverted data output	
19		GND	Module Ground	1
20		GND	Module Ground	1
21	CML-O	RX2-	Receiver inverted data output	
22	CML-O	RX2+	Receiver non-inverted data output	
23		GND	Module Ground	1
24	CML-O	RX4-	Receiver inverted data output	
25	CML-O	RX4+	Receiver non-inverted data output	

26		GND	Module Ground	1
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND	
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board	2
29		VCCTx	+3.3v Transmitter Power Supply	
30		VCC1	+3.3v Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	2
32		GND	Module Ground	1
33	CML-I	Tx3+	Transmitter non-inverted data input	
34	CML-I	Tx3-	Transmitter inverted data input	
35		GND	Module Ground	1
36	CML-I	Tx1+	Transmitter non-inverted data input	
37	CML-I	Tx1-	Transmitter inverted data input	
38		GND	Module Ground	1

Notes:

1. Module circuit ground is isolated from module chassis ground within the module.

2. Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15Vand3.6V.

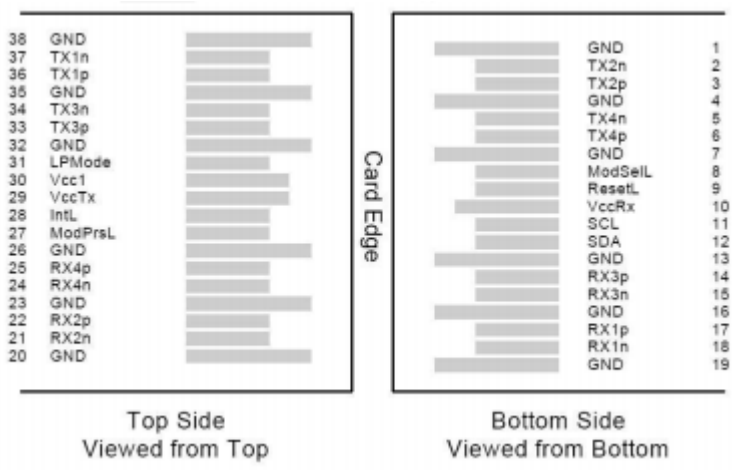


Figure2. Electrical Pin-out Details

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus.When the ModSelL is “High”, the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits untilthe module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signalwith the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

Gigalight QSFP28 ER4 operate in the low power mode (less than 1.5 W power consumption) This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pinis an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.

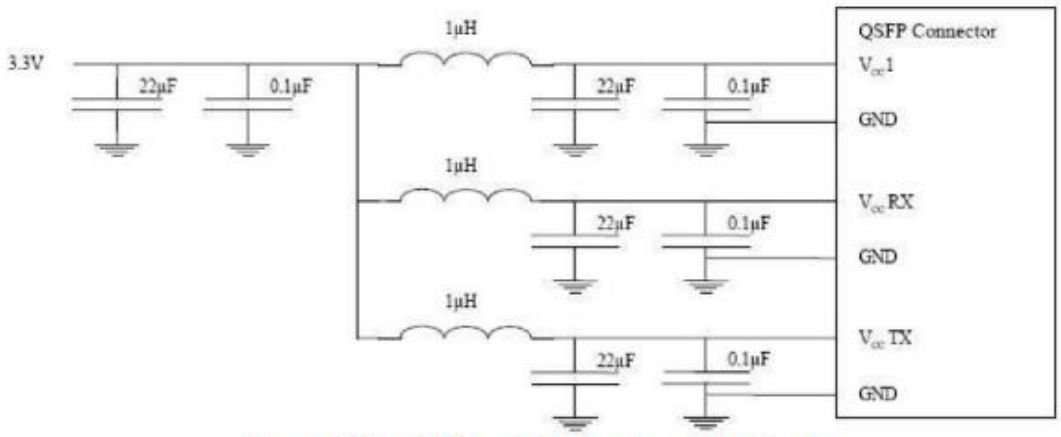


Figure3.Host Board Power Supply Filtering

Diagnostic Monitoring Interface

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Ma	Unit	Notes
Temperature monit	DMI_Temp	-3	+3	deg C	Over operating emperature
Supply voltag	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX ower	DMI_RX_Ch	-7	-22	dB	1
Channel Bias current monitor	DMI_Ibias_C h	- 10%	10%	mA	
Channel TX power	DMI_TX_Ch	-2.5	6.5	dB	1

Notes:

Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Digital diagnostics monitoring function is available on GNQ5L0C31. A 2-wire serial interface provides user to contact with module.

The structure of the memory is shown inFigure 5. The memory space is arranged into a lower, singlepage, address space of 128 bytes and multipleupper address space pages. This structure permits timely access to addresses in the lower page, such

asInterrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function.

The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

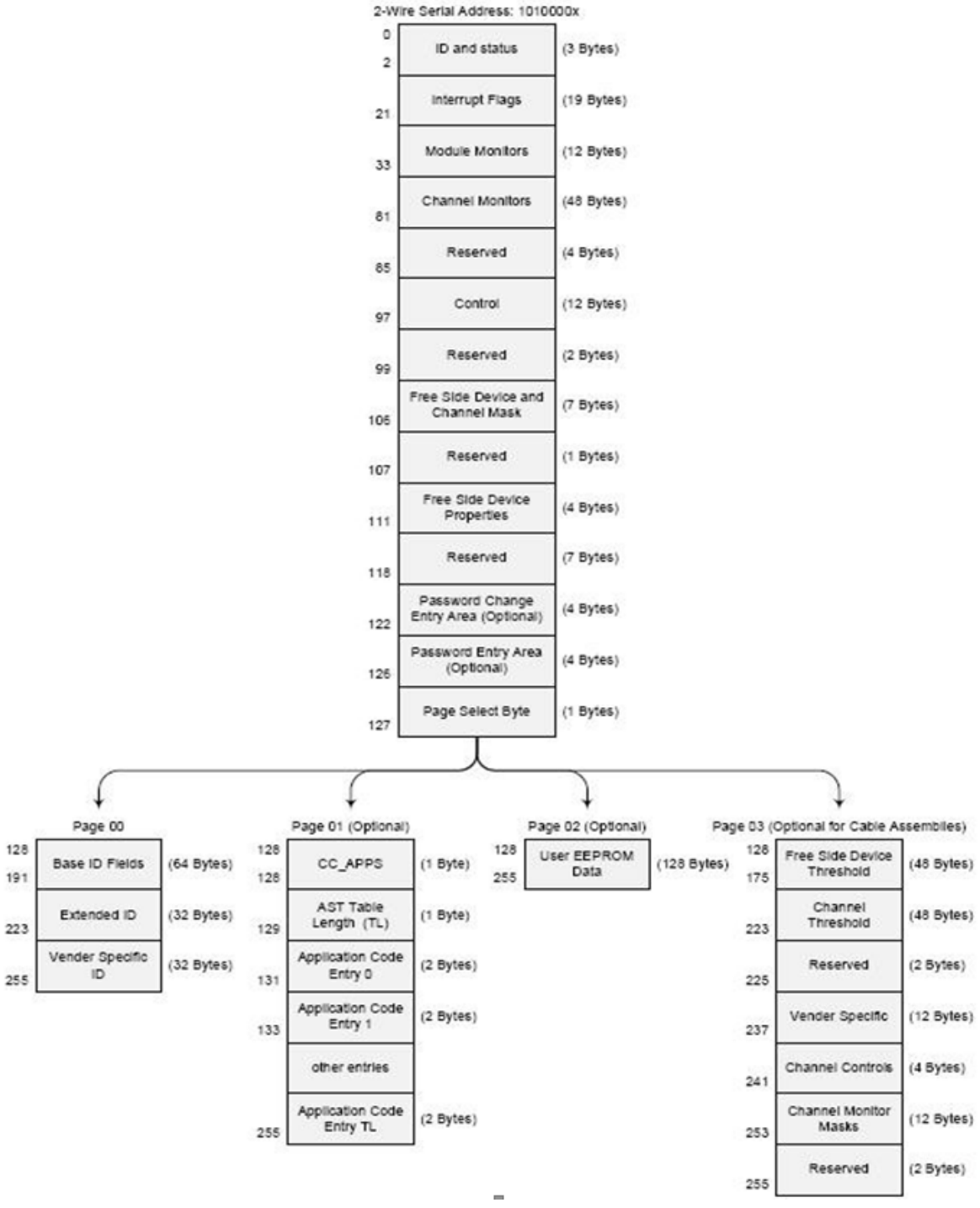


Figure5.QSFP Memory Map

Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on1, hot plug or rising edge of Reset until the module is fully functional2
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on1 until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on1 to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional2
LPMode Assert Time	ton_LPMode	100	μs	Time from assertion of LPMode (Vin:LPMode = Vih) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntLDeassert Time	toff_IntL	500	μs	Time from clear on read3 operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set4 until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared4 until associated IntlL operation resumes
ModSelL Assert Time	ton_ModSelL	100	μs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
ModSelLDeassert Time	toff_ModSelL	100	μs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set 4 until module power consumption enters lower Power Level
Power_over-ride or Power-set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared4 until the module is fully functional3

Note:

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.

2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted.

3. Measured from falling clock edge after stop bit of read transaction.

4. Measured from falling clock edge after stop bit of write transaction

Mechanical Dimensions

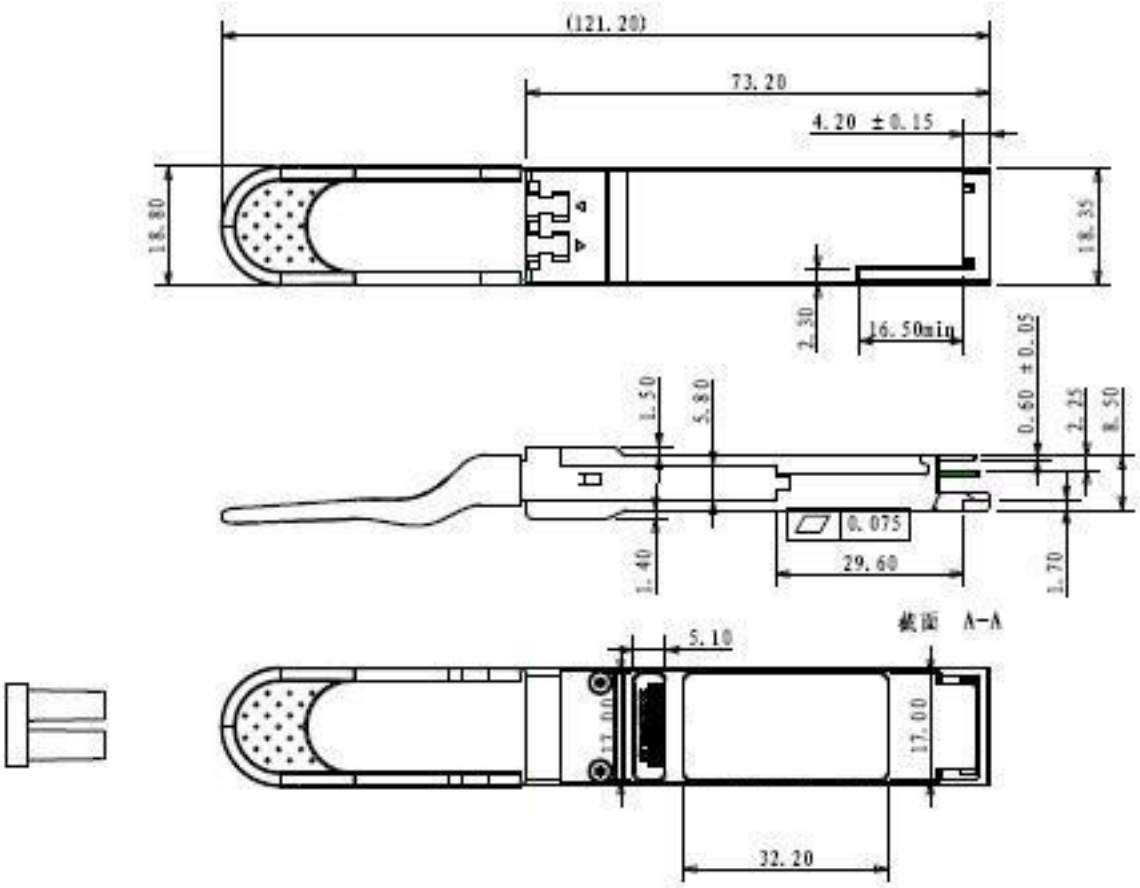


Figure6.Mechanical Specifications

Ordering information

Part Number	Product Description
GNQ5L0C31	QSFP28,100Gb/s, 1294 -1310nm ,SMF,40KM,DDM,LC connector, 0℃ ~ +70℃