

# 400G QSFP-DD to 2x200G QSFP56 Passive Copper Breakout Direct Attach Cable

## Features

- Compatible with IEEE 802.3bj and IEEE 802.3cd
- Supports aggregate data rates of 400Gb ps(PAM4)
- Optimized construction to minimize insertion loss and cross talk
- Pull-to-release slide latch design
- 28AWG through 30AWG cable
- Straight and break out assembly configurations available
- Customized cable braid termination limits EMI radiation
- Customizable EEPROM mapping for cable signature
- RoHS compliant

## Application

- Switches,servers and routers
- Data Center networks
- Storage area networks
- High performance computing
- Telecommunication and wireless infrastructure
- Medical diagnostics and networking
- Test and measurement equipment

## Standards Compliance

- 400G Ethernet(IEEE 802.3cd)

## Description

QSFP-DD\_2XQSFP56 passive copper cable assembly feature eight differential copper pairs,providing four data transmission channels at speeds up to 56Gb ps(PAM4) per channel,and meets 400G Ethernet and InfiniBand Enhanced Data Rate(EDR) requirements.Available in a broad rang of wire gages-from 28AWG through 30AWG-this 400G copper cable assembly features low insertion loss and low cross talk.

QSFP-DD\_2XQSFP56 uses PAM4 signals for transmission, which doubles the rate. However, there are more stringent requirements for cable insertion loss. For detailed requirements, please see High Speed Characteristics.

## High Speed Characteristics

Table1-High Speed Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential Impedance	TDR	90	100	110	n	
Insertion loss	SDD21	-16.06			dB	At 13.28 GHz
Differential Return Loss	SDD11 SDD22			See 1	dB	At 0.05 to 4.1 GHz
				See 2	dB	At 4.1 to 19 GHz
Common-mode to common-mode output return loss	SCC11 SCC22			-2	dB	At 0.2 to 19 GHz
Differential to common-mode return loss	SCD11			See 3	dB	At 0.01 to 12.89 GHz

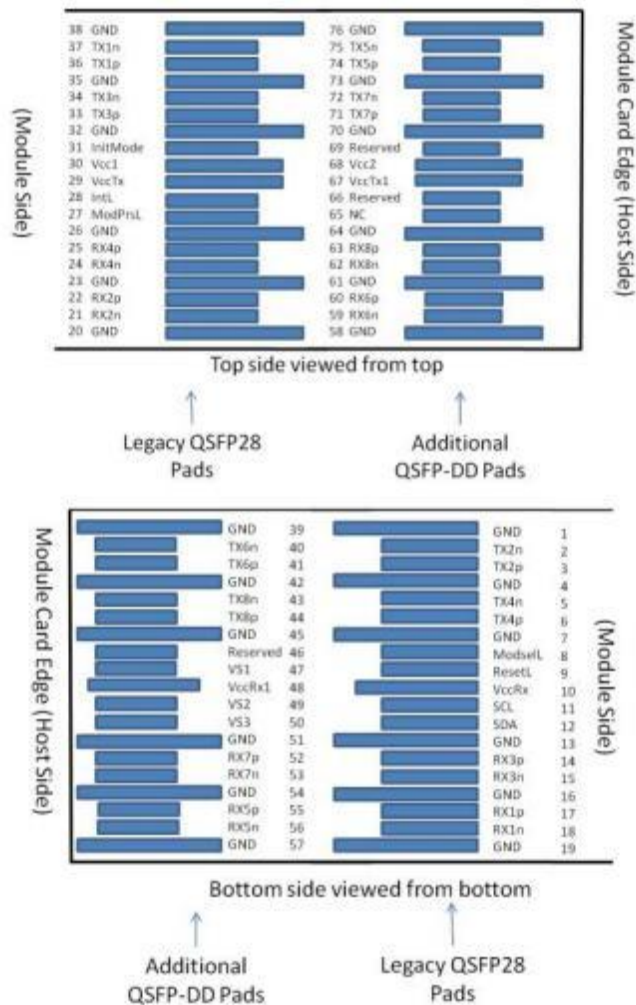
	SCD22			See 4		At 12.89 to 19 GHz
Differential to common Mode Conversion Loss	SCD21-IL			-10	dB	At 0.01 to 12.89 GHz
				See 5		At 12.89 to 15.7 GHz
				-6.3		At 15.7 to 19 GHz

## Notes:

- [1] Reflection Coefficient given by equation  $SDD11(dB) < -16.5 + 2 \times \sqrt{f}$ , with f in GHz
- [2] Reflection Coefficient given by equation  $SDD11(dB) < -10.66 + 14 \times \log_{10}(f/5.5)$ , with f in GHz
- [3] Reflection Coefficient given by equation  $SCD11(dB) < -22 + (20/25.78) \times f$ , with f in GHz
- [4] Reflection Coefficient given by equation  $SCD11(dB) < -15 + (6/25.78) \times f$ , with f in GHz
- [5] Reflection Coefficient given by equation  $SCD21(dB) < -27 + (29/22) \times f$ , with f in GHz

## Pin arrangement

### QSFP-DD end

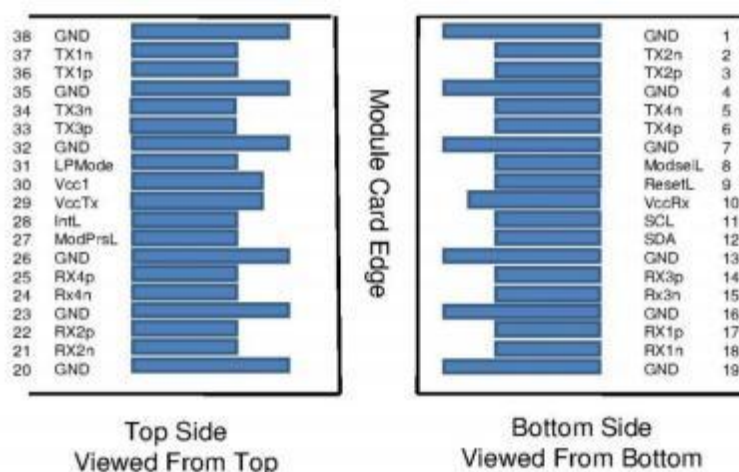


**QSFP-DD Pin Function Definition**
**Table2-Pin Description**

Pin	Logic	Symbol	Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		Vcc Rx	+3.3V Power Supply Receiver	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	
12	LVC MOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	1
23		GND	Ground	
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	1
26		GND	Ground	
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636)	2
29		VccTx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	1
32		GND	Ground	
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	1
35		GND	Ground	

36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	1
38		GND	Ground	1
39		GND	Ground	
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	1
42		GND	Ground	
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VS1	Module Vendor Specific 1	3
48		VccRx1	3.3V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future Use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69		Reserved	For future Use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

## QSFP56 end



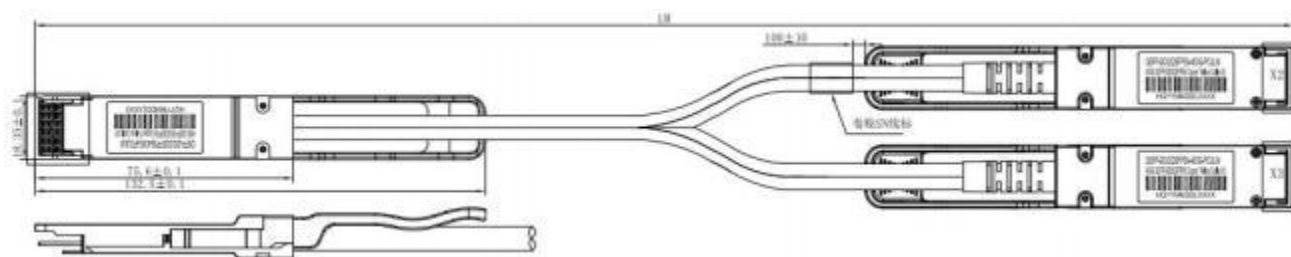
**Table3-Pin Description**

Pin	Symbols	Logic	Description	Notes
1	GND		Ground	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	
4	GND		Ground	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	
7	GND		Ground	
8	ModSelL	LVTTL-I	Module Select	
9	ResetL	LVTTL-I	Module Reset	
10	Vcc Rx		+3.3V Power Supply Receiver	2
11	SCL	LVCOMS-I/O	2-wire serial interface clock	
12	SDA	LVCOMS-I/O	2-wire serial interface data	
13	GND		Ground	
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	
15	Rx3n	CML-O	Receiver Inverted Data Output	
16	GND		Ground	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	
18	Rx1n	CML-O	Receiver Inverted Data Output	1
19	GND		Ground	1
20	GND		Ground	
21	Rx2n	CML-O	Receiver Inverted Data Output	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	
23	GND		Ground	
24	Rx4n	CML-O	Receiver Inverted Data Output	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	
26	GND		Ground	1

27	ModPrsL	LVTTTL-O	Module Present	
28	IntL	LVTTTL-O	Interrupt	
29	VccTx		+3.3V Power supply transmitter	2
30	Vcc1		+3.3V Power supply	2
31	LPMODE	LVTTTL-I	Low Power Mode	
32	GND		Ground	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	
34	Tx3n	CML-I	Transmitter Inverted Data Input	
35	GND		Ground	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	
37	Tx1n	CML-I	Transmitter Inverted Data Input	
38	GND		Ground	1

## Mechanical Specifications

The connector is compatible with the QSFP-DD and SFF-8436 specification.



Length (m)	Cable AWG
1.5	30
2.5	28

## Regulatory Compliance

Table4-Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.7	Class 1(>2000 Volts)
Electromagnetic Interference(EMI)	FCC Class B	Compliant with Standards
	CENELEC EN55022 Class B	
	CISPR22 ITE Class B	
RF Immunity( RFI)	IEC61000-4-3	Typically Show no Measurable Effect from a 10V/m Field Swept from 80 to 1000MHz
RoHS Compliance	RoHS Directive 2011/65/EU and it's Amendment Directives (EU) 2015/863	RoHS (EU) 2015/863 compliant
REACH Compliance	REACH Regulation (EC) No 1907/2006	REACH (EC) No 1907/2006 compliant