

400G QSFP-DD SR8 Optical Transceiver

Features

- Hot-pluggable QSFP-DD form factor
- Case temperature range of 0°C to +70°C
- Maximum link length of 100m on OM4 fiber
- with KP4 FEC
- +3.3V single power supply
- Power dissipation < 10W
- Operating case temp
- Commercial: 0°C to +70 °C
- MPO-16 APC connector
- RoHS compliant

Application

- 400G 100m on OM4 with FEC

Order Information

Table 1-Order Information

Part No.	Bit Rate (Gbps)	Laser (nm)	Distance note1	Fiber Type	DDMI	Connector	Tempnote2
400G QSFP-DD SR8	425	850	100m	MMF	YES	MPO 1x16 APC	0°C~+70°C

Note:

1.OM4 fiber, 70m for OM3 fiber, with KP4 FEC

2.Case Temperature

Absolute Maximum Ratings

Table2- Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Supply Voltage	V _{CC3}	-0.5	-	+3.6	V	
Storage Temperature	T _s	-40	-	+85	° C	
Operating Humidity	RH	+5	-	+85	%	1
Control Input Voltage	P _{RD} MG	+5	-	V _{CC} +0.5	V	1

Note:1 No condensation

Recommended Operating Conditions

Table 3- Recommended operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T _c	0	-	+70	° C	
Power Supply Voltage	V _{cc}	3.135	3.3	3.465	V	
Power Dissipation	P _d	-	-	10	W	

Note:

1.FEC provided by host system

2.FEC required on host system to support maximum distance

Electrical Characteristics

Table 4- Electrical Characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter						
Signaling rate (each lane)	SR	GBPS	26.5625 ± 100 ppm			
Differential data input voltage per lane	V _{in,pp,diff}	mV	900	-	-	
Differential termination mismatchal	-	%	-	-	10	
Single-ended voltage tolerance range	-	V	-0.4	-	3.3	
DC common mode voltage	-	mV	-350	-	2850	
Receiver						
Signaling rate (each lane)	SR	GBd	26.5625 ± 100 ppm			
Differential output voltage	-	mV	-	-	900	
Near-end ESMW (Eye symmetry mask width)	-	UI	0.265	-	-	
Near-end Eye height, differential (min)	-	mV	70	-	-	
Far-end ESMW (Eye symmetry mask width)	-	UI	0.2	-	-	
Far-end Eye height, differential (min)	-	mV	30	-	-	
Differential termination mismatch	-	%		-	10	
Transition time (min, 20% to 80%)	-	ps	9.5	-	-	
DC common mode voltage	-	mV	-350	-	2850	

Table 5-Optical Characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter						
Signaling rate (each lane)	SR	GBd	26.5625 ± 100 ppm			
Modulation format	-	-	PAM4			
Lane wavelength	λ	nm	840	850	860	
RMS spectral width	$\Delta \lambda$	nm	-	-	0.6	
Average launch power, each lane	-	dBm	-6.5	-	4	
Outer Optical Modulation Amplitude (OMA _{outer}), each lane	-	dBm	-4.5	-	3	1
Launch power in OMA _{outer} minus TDECQ, each lane	-	dBm	-5.9	-	-	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	-	dB	-	-	4.5	
Average launch power of OFF transmitter, each lane	-	dBm	-	-	-30	
Extinction ratio	-	dB	3	-	-	
Transmitter transition time, each lane	-	ps	-	-	34	
Optical return loss tolerance	-	dB	-	-	12	
Receiver						
Signaling rate (each lane)	SR	GBd	26.5625 ± 100 ppm			
Modulation format	-	-	PAM4			
Lane wavelength	λ	nm	840	850	860	
Damage threshold, each lane	PIN	dBm	5	-	-	
Average receive power, each lane	-	dBm	-8.4	-	4	
Receive power (OMA _{outer}), each lane	-	dBm	-	-	3	
Receiver sensitivity (OMA _{outer}), each lane	-	dBm	-	-	Max(6.5, SEC Q-7.9)	2
LOS Assert	-	dBm	-30	-	-10	
LOS De-Assert	-	dBm	-	-	-9	
LOS Hysteresis	-	dB	0.5	-	-	

Note:

- Even if the TDECQ < 1.4 dB, the OMA_{outer} (min) must exceed this value.
- Bit Error Ratio < 2.4x10⁻⁴, Pattern PRBS31Q

Recommended Interface

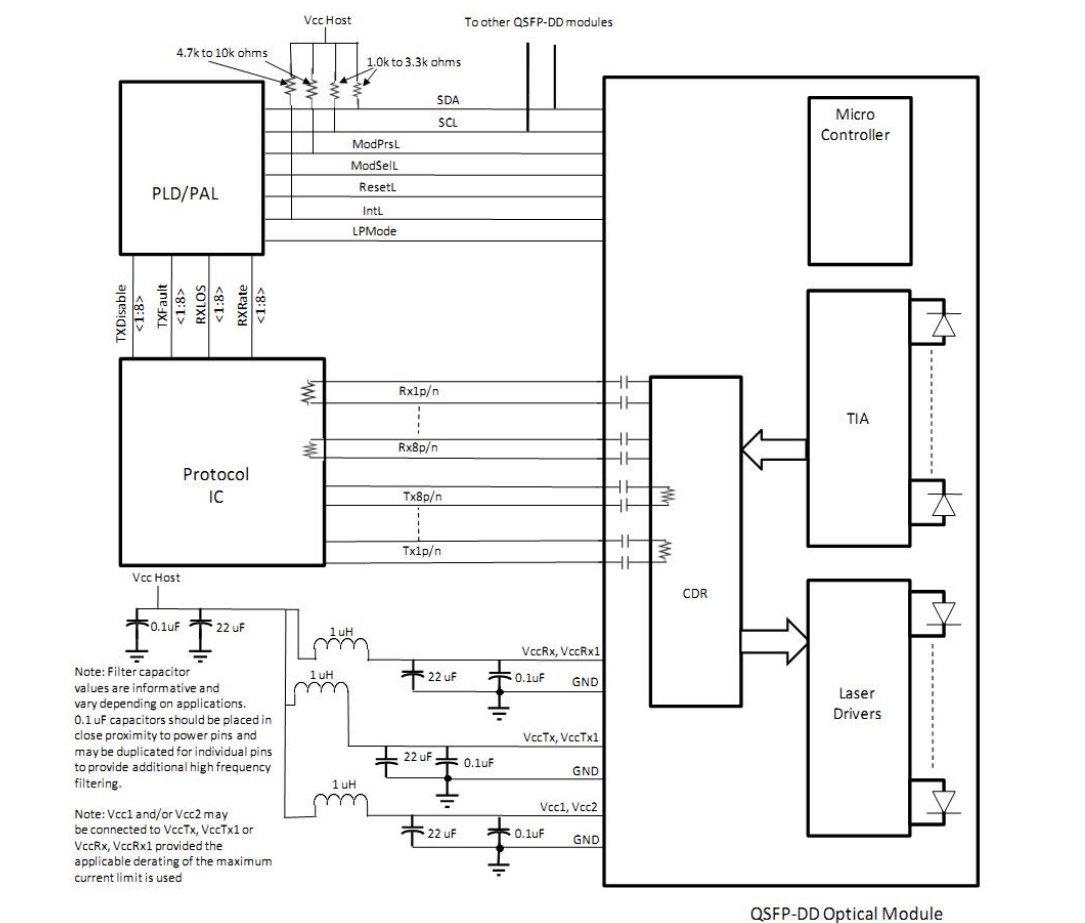


Figure 1, Recommended Interface Circuit

Pin arrangement

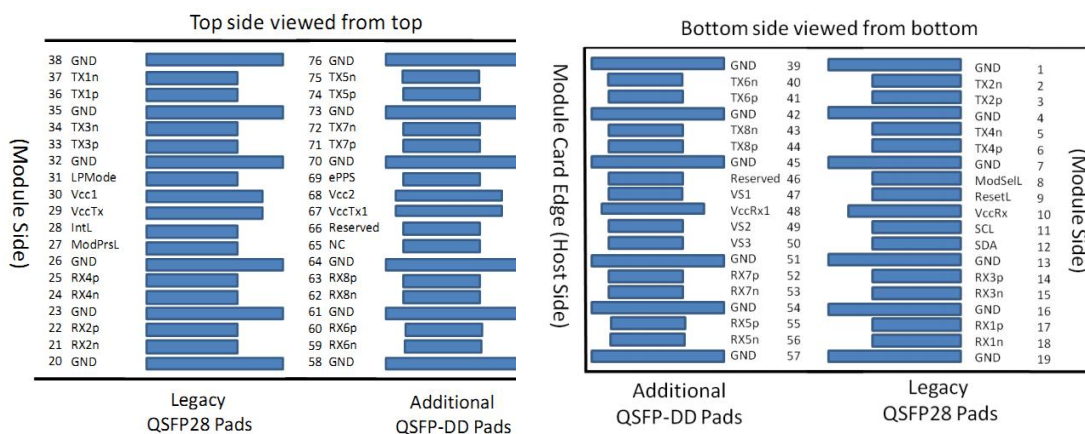


Figure 2, Pin View

Table 6-Pin Function Definitions

Pad	Logic	Symbol	Description	Plug Sequence ⁴	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-0	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-0	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-0	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-0	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-0	Rx2n	Receiver Inverted Data Output	3B	
22	CML-0	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-0	Rx4n	Receiver Inverted Data Output	3B	
25	CML-0	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-0	ModPrsL	Module Present	3B	
28	LVTTL-0	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2

30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMODE	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-0	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-0	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-0	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-0	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-0	Rx6n	Receiver Inverted Data Output	3A	
60	CML-0	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1

62	CML-0	Rx8n	Receiver Inverted Data Output	3A	
63	CML-0	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Timeclock input Protocol(PTP) reference	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note: 1. Circuit ground is internally isolated from chassis ground.

Memory Map

Compatible with QSFP-DD CMIS rev 4.0.

Optical interface arrangement

The optical port is a male MPO connector receptacle, with fiber lane assignments as shown in Figure 3

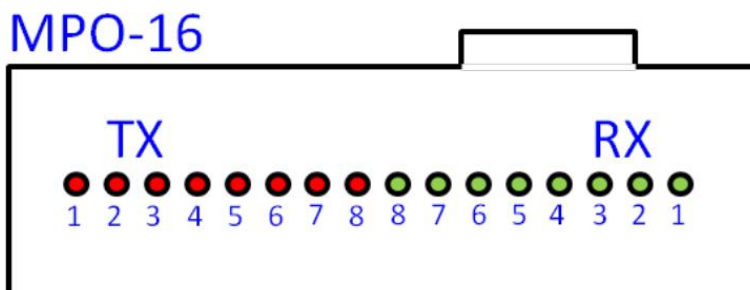


Figure 3,Optical interface arrangement. Lens upwards.

Mechanical

QSFP-DD SR8 transceivers are compatible with the QSFP-DD Type 2 Specification for pluggable form factor modules.

Unit mm

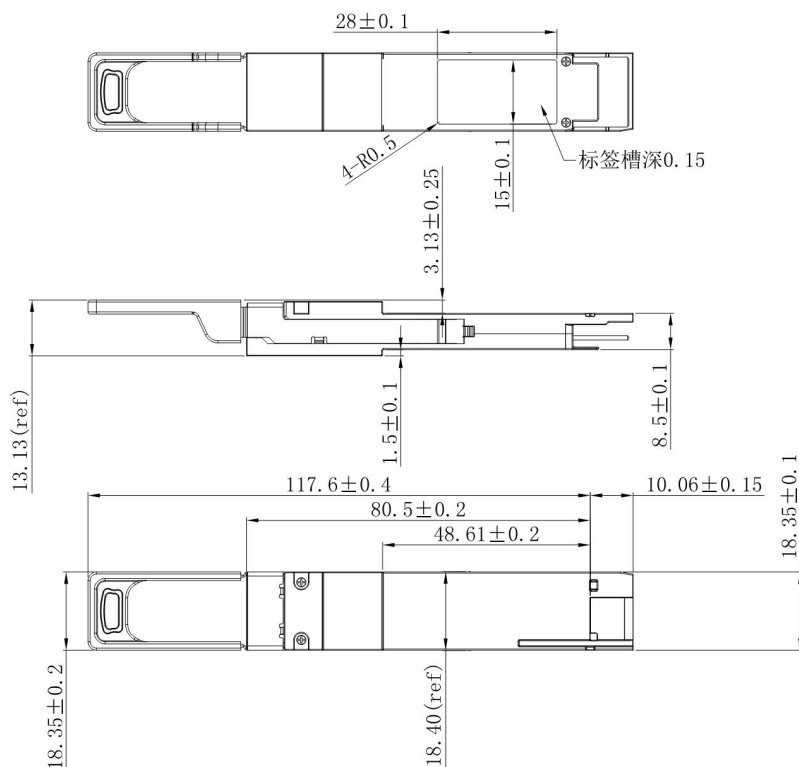


Figure 5,Mechanical Diagram