

400G OSFP SR4 Optical Transceiver

Features

- Up to 50Gbps data rate per channel by PAM4 modulation
- Hot-pluggable OSFP form factor
- Maximum link length of 50m on OM4 fiber with FEC
- +3.3V single power supply
- Power dissipation < 9W
- Operating case temp Commercial: 0°C to +70 °C
- MPO-12 APC connector
- RoHS compliant
- Pre-FEC BER $\leq 1E-8$ in the switcher equipment
- self-loopback test

Application

- Application case 1, 1x400G VR4, 1 of 400G per port point to point connections
- Application case 2, 4x100G VR, 4 of 100G per channel breakout connections

Order Information

Table 1-Order Information

Part No.	Bit Rate (Gbps)	Laser (nm)	Distance note1	Fiber Type	DDMI	Connector	Tempnote2
400G OSFP SR4	425.0	850	50m	MMF	YES	MPO 1x12 APC	0°C~+70°C

Note:

1.OM4 fiber, 30m for OM3 fiber, with FEC

2.Case Temperature

Absolute Maximum Ratings

Table2- Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Supply Voltage	Vcc3	-0.5	-	+3.6	V	
Storage Temperature	Ts	-40	-	+85	° C	
Operating Humidity	RH	0	-	+85	%	1
Control Input Voltage	VI	-0.3	-	VCC+0.5	V	1

Note:1 No condensation

Recommended Operating Conditions

Table 3- Recommended operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	TC	0	-	+70	° C	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Dissipation	Pd	-	-	9	W	
Supply Current	Icc	-	-	2870	mA	
Pre-FEC Bit Error Ratio	-	-	-	2.4x10-4	-	
Post-FEC Bit Error Ratio	-	-	-	1x10-12	-	1
Link Distance (OM4)	-	2	-	50	m	2
Link Distance (OM3)	-	2	-	30	m	

Note:

1.FEC provided by host system

2.FEC required on host system to support maximum distance

Electrical Characteristics

Table 4- Electrical Characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter						
Signaling Rate per Lane	SR	Gbd	53.125 ± 100 ppm			
Modulation format	-	-	PAM4			
Differential pk-pk input Voltage tolerance	Vin,pp,diff	mV	750	-	-	
Peak-to-peak AC common-mode voltage tolerance Low-frequency Full-band	VCMLF VCMFB	mV	32 80	-	-	
Differential-mode to common-mode return loss	RLcd	dB	IEEE 803.3ck Equation (120G-2)	-	-	
Module stressed input tolerance	-	-	IEEE802.3ck 120G.3.4.3			
Effective return loss	ERL	dB	8.5			
Differential termination mismatchal	-	%	-	-	10	
Single-ended voltage tolerance range	-	V	-0.4	-	3.3	
DC common-mode voltage tolerance Upper limit Lower limit	-	mV	2850 -350			
Receiver						
Signaling Rate per Lane	SR	Gbd	53.125 ± 100 ppm			
Modulation format	-	-	PAM4			

Peak-to-peak AC common-mode voltage Low-frequency Full-band	VCMLF VCMFB	mV	-	-	32 80	
Differential output Voltage (Long mode)	-	mV	-	-	845	
Differential output Voltage (Short mode)	-	mV	-	-	600	
Eye height	-	mV	15	-	-	
Vertical eye closure	VEC	mV	-	-	12	
Common-mode to differential-mode return loss	RLdc	dB	IEEE 803.3ck Equation (120G-1)	-	-	
Differential Termination Mismatch	-	%	-	-	10	
Transition Time	-	ps	8.5	-	-	
DC common mode Voltage tolerance Upper limit Lower limit	-	mV	2850 -350			

Table 5-Optical Characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter						
Signaling Rate per Lane	SR	Gbd	53.125 ± 100 ppm			
Modulation format	-	-	PAM4			
Center wavelength	CW	nm	842	-	948	
RMS Spectral Width	SW	dBm	-	-	0.65	1
Average Launch Power per Lane	AOP	dBm	-4.6	-	4.0	
Outer Optical Modulation Amplitude (OMA _{outer}), each lane (min) For max(TECQ,TDECQ)≤1.8dB For 1.8<max(TECQ,TDECQ)≤4.4dB	TxOMA	dBm	-2.6 -4.4+max(TECQ, TDECQ)	-	3.5	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	dB	-	-	4.4	
Transmitter eye closure for PAM4,each lane	TECQ	dB	-	-	4.4	
Overshoot/undershoot	-	%	-	-	29	
Transmitter power excursion,each lane	-	dBm	-	-	2.3	
Transition Time	Tt	ps	-	-	17	
Average Launch Power of OFF Transmitter, each lane	TOFF	dBm	-	-	-30	
RIN _{14OMA}	RIN	dB/H z	-	-	-132	
Extinction Ratio, each lane	ER	dB	2.5	-	-	

Optical Return Loss Tolerance	ORL	dB	-	-	14	
Encircled flux	-	dBm	$\geq 86\%$ at 19 μ m $\leq 30\%$ at 4.5 μ m			2
Receiver						
Signaling Rate per Lane	SR	Gbd	53.125 \pm 100 ppm			
Modulation format	-	-	PAM4			
Wavelength	W	nm	842	-	948	
Damage Threshold, average optical power, each lane	DT	dBm	5	-	-	3
Average Receive Power, each lane	RXPx	dBm	-6.3	-	4	4
Receive Power (OMA) per Lane	RxOMA	dBm	-	-	3.5	
Receiver Reflectance	Rfl	dB	-	-	-15	
Receiver Sensitivity (OMAuter), each lane For TECQ \leq 1.8dB For 1.8<TECQ \leq 4.4dB	SEN	dBm	-	-	-4.4 -6.2+T ECQ	5
LOS Assert	LOSA	dBm	-15	-	-	
LOS De-assert	LOSD	dBm	-	-	-9.2	
LOS Hysteresis	LOSH	dB	0.5	-	-	
OMAuter of each aggressor lane	-	dBm	-	3.5	-	

Note:

1. RMS spectral width is the standard deviation of the spectrum
2. If measured into type A1a.2 or type A1a.3, or A1a.4, 50 μm fiber, in accordance with IEC 61280-1-4
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength.
5. A received power below this value cannot be compliant; however, a value above this does not ensure Receiver sensitivity (OMAuter) is informative and is defined for a transmitter with a value of TECQ up to 4.4 dB

Digital Diagnostic Specifications

Table 6-Digital Diagnostic Characteristics

Parameter	Symbol	Unit	Min	Max	Notes
Temperature monitor absolute error	DMI_Temp	degC	-3	3	Over operating temperature range
Supply voltage monitor absolute error	DMI_VCC	V	-0.1	0.1	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	dB	-3	3	1
Channel Bias current monitor	DMI_Ibias_Ch	mA	-10%	10%	
Channel TX power monitor absolute error	DMI_TX_Ch	dB	-3	3	1

Notes:

1. Due to measurement accuracy of different multi-mode fibers, there could be an additional
2. +/-1 dB fluctuation, or a +/- 3 dB total accuracy

Recommended Interface

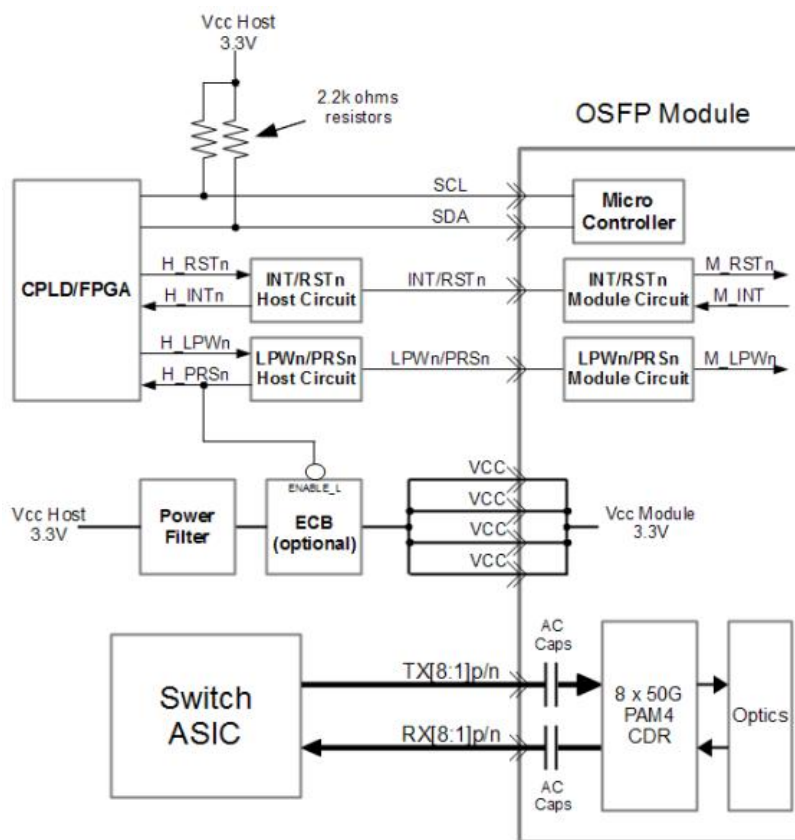


Figure 1, Recommended Interface Circuit

Pin arrangement

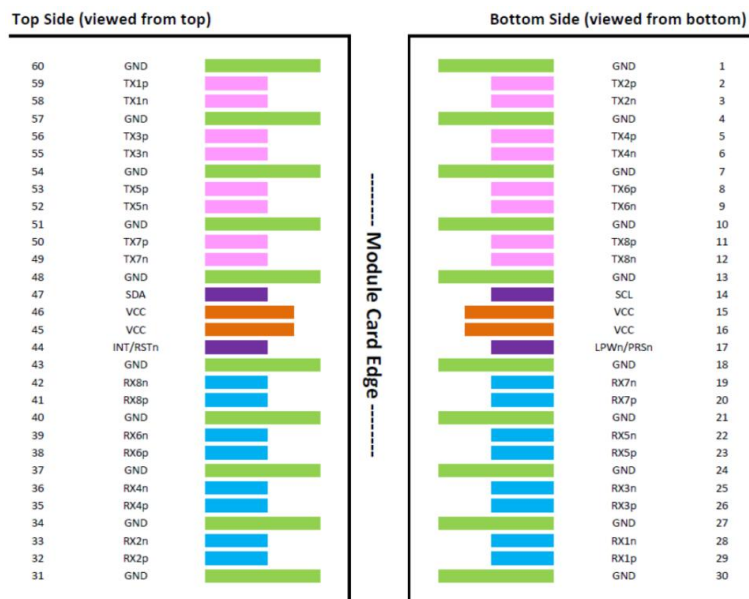


Figure 2, Pin View

Table 7-Pin Function Definitions

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-1	nput from Host	3	
3	TX2n	Transmitter Data Inverted	CML-1	nput from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-1	nput from Host	3	
6	TX4n	Transmitter Data Inverted	CML-1	nput from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-1	nput from Host	3	
9	TX6n	Transmitter Data Inverted	CML-1	nput from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-1	nput from Host	3	
12	TX8n	Transmitter Data Inverted	CML-1	nput from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface dock	LVC MOS- /0	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode/Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-0	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-0	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-0	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-0	Output to Host	3	

26	RX3p	Receiver Data Non-Inverted	CML-0	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-0	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-0	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-0	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-0	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-0	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-0	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-0	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-0	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-0	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-0	Output to Host	3	
43	GND	Ground			1	
44	NT/RSTn	Module Interrupt/Module Reset	Multi-Level	Bi-directional	3	See pin description or required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VcC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interfacedata	LVC MOS-1/0	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-	nput from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-	nput from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-	nput from Host	3	

53	TXSp	Transmitter Data Non-Inverted	CML-	nputfrom Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-	nputfrom Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-	nputfrom Host	3	
57	GND	Ground			1	
58	TXIn	Transmitter Data Inverted	CML-	nputfrom Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-	nputfrom Host	3	
60	GND	Ground			1	

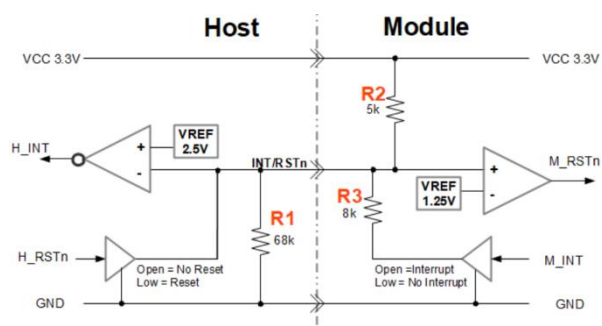


Figure 2,INT/RSTn circuit

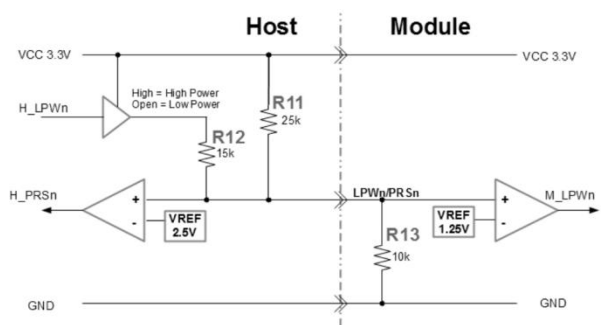


Figure 3,LPWn/PRSn circuit

Memory Map

Compatible with CMIS rev 5.2.

Optical interface arrangement

The optical port is a male MPO connector receptacle, with fiber lane assignments as shown in Figure 3

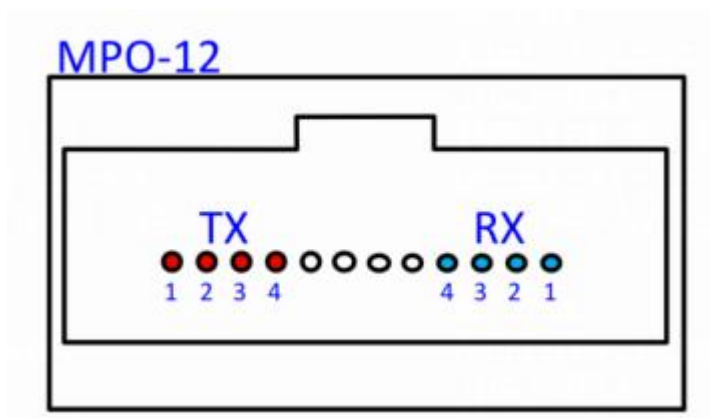


Figure 3,Optical interface arrangement.

Mechanical

400G SR4 OSFP transceivers are compatible with OSFP Module Specification Rev5.0 for pluggable form factor module.

Unit mm