

# 800GBASE-SR8 OSFP 850nm 50m Dual MTP/MPO-12/APC DOM Transceiver

#### **Standards**

- Compliant to OSFP MSA 5.0
- Compliant with CMIS 5.1
- 8x106. 25Gb/s Electrical Interface (800GAUI-8)
- Maximum Power Consumption 16W
- Single +3.3V Power Supply
- Case Temperature Range:  $0 \sim +70^{\circ}$ C
- RoHS 2.0 Complaint

#### **Features**

- Up to 106.25 Gbps Data Rate Per Channel by PAM4 Modulation
- Support 800GAUI-8 Electrical Interface
- Integrated 850nm VCSEL Array and PD Array
- DDM Function Implemented
- Hot-pluggable
- Single +3.3V Power Supply

## **Application**

- Data Centers and Cloud
- Networks

### **Description**

The 800GBASE-SR8 OSFP Optical Transceiver Module is designed for use in 800Gb/s systems throughput up to 30m over OM3 or 50m over OM4 multimode fiber (MMF) using a wavelength of 850nm via dual MTP/MPO-12 connectors.

Digital diagnostics functions are also available via the I2C interface, as specified by the OSFP MSA, to allow access to real-

time operating parameters. With these features, this easy to install, hot swappable transceiver is suitable to be used in various applications, such as data centers, high-performance computing networks, enterprise core and distribution layer applications.

#### **Product Specifications**

#### I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	TSTG	-40	85	$^{\circ}$ C
Supply Voltage	VCC	0	4	V
Relative Humidity (Non-condensing)	RH	5	85	%

#### **Order Information**

#### **Table 1-Order Information**

Part No.	Bit Rate (Gbps)	Laser (nm)	Distanc e note1	Fiber Type	DDMI	Connector	Tempnote2
400G QSFP-DD SR8	425	850	100m	MMF	YES	MPO 1x16 APC	0℃~+70℃



Note:
1.OM4 fiber, 70m for OM3 fiber, with KP4 FEC
2.Case Temperature

# **II. Recommended Operating Conditions**

Parameter	Symbol	Min.	Max.	Unit
Case Temperature- Operating	TCASE	0	70	$^{\circ}$
Supply Voltage	VCC	3.135	3.465	V
Power Consumption	PDISS		16	W
Pre-FEC Bit Error Ratio			2.4x10 <sup>-4</sup>	
Link Distance over OM3		0.5	30	М
Link Distance over OM4		0.5	50	M

## **III. Optical Characteristics**

Parameter	Min.	Typical	Max.	Unit
	Transmitter			
Signaling Rate, Each Lane	53	.125 ± 100 ppi	m	GBd
Lane Wavelength Range		850		nm
RMS Spectral Width			0.6	nm
Modulation Format		PAM	[4	
Average Optical Power Per Lane	-4.6		4	dBm
Outer Optical Modulat	tion Amplitude (	OMAouter), Eac	h Lane	
for TDECQ≤1.8dB	-2.6		3.5	dBm
for 1.8 <tdecq≤4.4db< td=""><td>-4.4+TDECQ</td><td></td><td>3.5</td><td>dBm</td></tdecq≤4.4db<>	-4.4+TDECQ		3.5	dBm
Outer Optical Modulation Amplitude (OMAouter), Each Lane				
for TECQ≤1.8dB	-2.6		3.5	dBm
for 1.8 <tecq≤4.4db< td=""><td>-4.4+TECQ</td><td></td><td>3.5</td><td>dBm</td></tecq≤4.4db<>	-4.4+TECQ		3.5	dBm
Transmitter and Dispersion Eye Closure for PAM4, Each Lane			4.4	dB
Transmitter Eye Closure for PAM4 (TECQ), Each Lane			4.4	dB
ExtinctionRatio	2.5			dB
Transmitter Excursion, Each Lane			2	dB
Transmitter Transition Time, Each Lane			17	ps
Parameter	Min.	Typical	Max.	Unit
Average Launch Power Per Lane @ TX Off State			-30	dBm
Relative Intensity Noise12 (OMA)			-131	dB/Hz
Optical Return Loss Tolerance			12	dB
Encircled Flux	>=86% at	19μm <=30%	at 4.5µm	dB



Receiver					
Signaling Rate Each Lane	5	53. $125 \pm 100$ ppm			
Lane Wavelength Range		850		nm	
Modulation Format		PAM	[4		
Damage Threshold	5			dBm	
Average Receive Power, Each Lane	-6.4		4	dBm	
Receiver Power, Each Lane (OMA)			3.5	dBm	
Receiver Sensitivity Each Lane (OMAouter)					
for TECQ≤1.8dB			-4.6	dBm	
for 1.8 <tecq≤4.4db< td=""><td></td><td></td><td>-6.4+TECQ</td><td>dBm</td></tecq≤4.4db<>			-6.4+TECQ	dBm	
Receiver Reflectance			-12	dB	
Stressed Receiver Sensitivity (OMAouter), Each Lane			-2	dBm	
Stressed Conditions for Stress Receiver Sensitivity					
Stressed Eye Closure for PAM4 (SECQ), Lane under Test		4.4		dB	
OMAouter of Each Aggressor Lane		3.5		dBm	

# IV. High Speed Electrical Signals

Parameter	Min.	Тур.	Max.	Unit
Transmitter Elect	trical Input Chara	cteristics at T	ГР1	
Signaling Rate, Per Lane		53.125		GBd
Differential Pk-pk Input Voltage Tolerance	900			mV
Common-mode to Differential Return Loss	802.3ck Equation(120G-1)			
Effective Return Loss	TBD			
Differential Termination Mismatch			10	%
Module Stressed Input Test	See 120G.3.4.1			
Single-ended Voltage Tolerance Range	-0.4		3.3	V
DC Common-mode Voltage	-350		2850	mV
Receiver Electric	cal Output Charac	cteristics at T	P4	
Signaling Rate Per Lane		53.125		GBd
AC common-mode Output Voltage(RMS)			17.5	mV
Differential Peak-to-peak Output Voltage			900	dB
Near-end ESMW (Eye Symmetry Mask Width)		TBD		UI
Near-end Eyeheight, Differential	24			mV
Parameter	Min.	Тур.	Max.	Unit
Near-end Vertical Eye Closure			7.5	dB



Far-end ESMW (Eye Symmetry Mask Width)		TBD		
Far-end Eyeheight, Differential	24			mV
Far-end Vertical Eye Closure			7.5	dB
Far-end Pre-cursor ISI Ratio		TBD		UI
Common Mode to Differential Conversion Return Loss	802.3ck 120G-1			dB
Effective Return Loss	TBD			dB
Differential Termination Mismatch			10	%
Transition Time (min,20%to80%)		TBD		ps
DC Common Mode Voltage	-350 2850			mV

# V. Low Speed Electrical Signals

Parameter	Symbol	Min.	Max.	Unit	Condition
agr. 1ap.	VOL	0	0.4	V	IOL(max)=3.0mA for
SCL and SDA	VOH	Vcc-0.5	Vcc+0.3	V	Fast Mode, 20mA for Fast-mode Plus
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
SCL and SDA	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O Pin	Ci		14	pF	
Parameter	Symbol	Min.	Max.	Unit	Condition
Total Bus Cpacitive Load	Cb		100	pF	3.0k Ohms Pull up Resistor, Max
for SCL and SDA			200	pF	1.6k Ohms Pull up Resistor, Max
LPMode/TxDis, Reset and	VIL	-0.3	0.8	V	II'   105   105   105
ModeSeIL	VIH	2	Vcc+0.3	V	Iin  = 125uA for Vin < VCC</td
	VOL	0	0.4	V	IOL=2.0mA
IntL/RxLOS	VOH	VCC-0.5	VCC+0.3	V	10k Ohms Pull-up to Host Vcc
	VOL	0	0.4	%	IOL=2.0mA
ModPrsL	VOH			dB	ModPrsL can be implemented as a short-circuit to GND on the module



## VI. Pin Definition

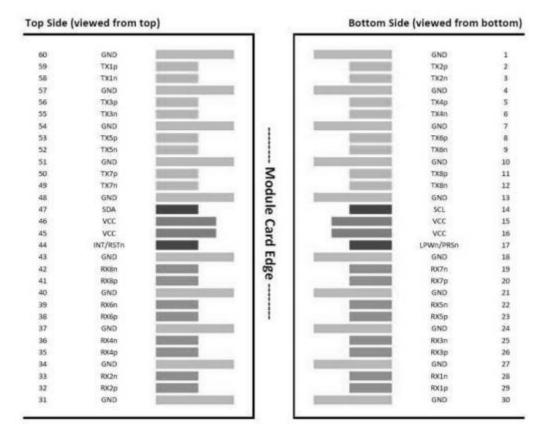


Figure 1. OSFP800 800G Contact Assignment

## VII. Pin Description

Pin	Symbol	Logic	Description	Note
1	GND		Ground	
2	TX2p	CML-I	Transmitted Data Non-Inverted	
3	TX2n	CML-I	Transmitted Data Inverted	
4	GND		Ground	
5	TX4p	CML-I	Transmitted Data Non-Inverted	
6	TX4n	CML-I	Transmitted Data Inverted	
7	GND		Ground	
8	TX6p	CML-I	Transmitted Data Non-Inverted	
9	TX6n	CML-I	Transmitted Data Inverted	
10	GND		Ground	
11	TX8p	CML-I	Transmitted Data Non-Inverted	
12	TX8n	CML-I	Transmitted Data Inverted	
13	GND		Ground	
14	SCL	LVCMOS-I/O	2-wire Serial Interface Clock	1
15	VCC		+3.3V Power	



17	1.6	TIGG		. 2 277 D	
18         GND         Ground           19         RX7n         CML-O         Receiver Data Inverted           20         RX7p         CML-O         Receiver Data Inverted           21         GND         Ground           22         RX5n         CML-O         Receiver Data Inverted           23         RX5p         CML-O         Receiver Data Non-Inverted           24         GND         Ground           Pin         Symbol         Logic         Description         Note           25         RX3n         CML-O         Receiver Data Inverted         CML-O         Receiver Data Inverted           26         RX3p         CML-O         Receiver Data Inverted         CML-O         Receiver Data Inverted           27         GND         Ground         Ground         Ground         GROUND         Ground           31         GND         Ground         GROUND <td>16</td> <td>VCC</td> <td></td> <td>+3.3V Power</td> <td></td>	16	VCC		+3.3V Power	
19         RX7p         CML-O         Receiver Data Inverted           20         RX7p         CML-O         Receiver Data Non-Inverted           21         GND         Ground           22         RX5n         CML-O         Receiver Data Inverted           23         RX5p         CML-O         Receiver Data Non-Inverted           24         GND         Ground           Pin         Symbol         Logic         Description         Note           25         RX3n         CML-O         Receiver Data Inverted           26         RX3p         CML-O         Receiver Data Inverted           27         GND         Ground           28         RX In         CML-O         Receiver Data Inverted           29         RX Ip         CML-O         Receiver Data Non-Inverted           30         GND         Ground           31         GND         Ground           32         RX2p         CML-O         Receiver Data Inverted           33         RX2n         CML-O         Receiver Data Inverted           34         GND         Ground           35         RX4p         CML-O         Receiver Data Non-Inverted <td< td=""><td></td><td></td><td>Multi-Level</td><td></td><td>2</td></td<>			Multi-Level		2
20         RX7p         CML-O         Receiver Data Non-Inverted           21         GND         Ground           22         RX5n         CML-O         Receiver Data Inverted           23         RX5p         CML-O         Receiver Data Inverted           24         GND         Ground           Pin         Symbol         Logic         Description         Note           25         RX3n         CML-O         Receiver Data Inverted           26         RX3p         CML-O         Receiver Data Non-Inverted           27         GND         Ground           28         RX In         CML-O         Receiver Data Inverted           29         RX Ip         CML-O         Receiver Data Non-Inverted           30         GND         Ground           31         GND         Ground           32         RX2p         CML-O         Receiver Data Inverted           33         RX2p         CML-O         Receiver Data Inverted           34         GND         Ground           35         RX4p         CML-O         Receiver Data Non-Inverted           36         RX4n         CML-O         Receiver Data Non-Inverted					
21         GND         Ground           22         RX5n         CML-O         Receiver Data Inverted           23         RX5p         CML-O         Receiver Data Inverted           24         GND         Ground         Note           24         GND         Ground         Note           25         RX3n         CML-O         Receiver Data Inverted           26         RX3p         CML-O         Receiver Data Inverted           27         GND         Ground           28         RX In         CML-O         Receiver Data Inverted           29         RX 1p         CML-O         Receiver Data Non-Inverted           30         GND         Ground           31         GND         Ground           32         RX2p         CML-O         Receiver Data Inverted           34         GND         Ground           35         RX4p         CML-O         Receiver Data Inverted           36         RX4n         CML-O         Receiver Data Non-Inverted           37         GND         Ground           38         RX6p         CML-O         Receiver Data Inverted           40         GND         Ground					
22         RX5p         CML-O         Receiver Data Inverted           23         RX5p         CML-O         Receiver Data Non-Inverted           24         GND         Ground           Pin         Symbol         Logic         Description         Note           25         RX3n         CML-O         Receiver Data Inverted           26         RX3p         CML-O         Receiver Data Non-Inverted           27         GND         Ground           28         RX In         CML-O         Receiver Data Inverted           29         RX Ip         CML-O         Receiver Data Non-Inverted           30         GND         Ground           31         GND         Ground           32         RX2p         CML-O         Receiver Data Inverted           34         GND         Ground           35         RX4p         CML-O         Receiver Data Inverted           36         RX4n         CML-O         Receiver Data Inverted           37         GND         Ground           38         RX6p         CML-O         Receiver Data Inverted           40         GND         Ground           41         RX8p         C			CML-O		
23         RX5p         CML-O         Receiver Data Non-Inverted           24         GND         Ground           Pin         Symbol         Logic         Description         Note           25         RX3n         CML-O         Receiver Data Inverted           26         RX3p         CML-O         Receiver Data Inverted           27         GND         Ground           28         RX 1n         CML-O         Receiver Data Inverted           29         RX 1p         CML-O         Receiver Data Inverted           30         GND         Ground           31         GND         Ground           32         RX2p         CML-O         Receiver Data Inverted           34         GND         Ground           35         RX4p         CML-O         Receiver Data Inverted           36         RX4n         CML-O         Receiver Data Inverted           37         GND         Ground           38         RX6p         CML-O         Receiver Data Inverted           40         GND         Ground           41         RX8p         CML-O         Receiver Data Inverted           42         RX8n         CML-O <td></td> <td></td> <td></td> <td></td> <td></td>					
24         GND         Ground           Pin         Symbol         Logic         Description         Note           25         RX3n         CML-O         Receiver Data Inverted           26         RX3p         CML-O         Receiver Data Non-Inverted           27         GND         Ground           28         RX 1n         CML-O         Receiver Data Inverted           29         RX 1p         CML-O         Receiver Data Non-Inverted           30         GND         Ground           31         GND         Ground           32         RX2p         CML-O         Receiver Data Non-Inverted           34         GND         Ground           35         RX4p         CML-O         Receiver Data Inverted           36         RX4n         CML-O         Receiver Data Inverted           37         GND         Ground           38         RX6p         CML-O         Receiver Data Inverted           40         GND         Ground           41         RX8p         CML-O         Receiver Data Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Gr					
Pin         Symbol         Logic         Description         Note           25         RX3n         CML-O         Receiver Data Inverted           26         RX3p         CML-O         Receiver Data Inverted           27         GND         Ground           28         RX In         CML-O         Receiver Data Inverted           29         RX Ip         CML-O         Receiver Data Non-Inverted           30         GND         Ground           31         GND         Ground           32         RX2p         CML-O         Receiver Data Inverted           34         GND         Ground           35         RX4p         CML-O         Receiver Data Inverted           36         RX4n         CML-O         Receiver Data Inverted           37         GND         Ground           38         RX6p         CML-O         Receiver Data Inverted           40         GND         Ground           41         RX8p         CML-O         Receiver Data Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi			CML-O		
25         RX3n         CML-O         Receiver Data Inverted           26         RX3p         CML-O         Receiver Data Non-Inverted           27         GND         Ground           28         RX In         CML-O         Receiver Data Inverted           29         RX Ip         CML-O         Receiver Data Non-Inverted           30         GND         Ground           31         GND         Ground           32         RX2p         CML-O         Receiver Data Non-Inverted           33         RX2n         CML-O         Receiver Data Inverted           34         GND         Ground           35         RX4p         CML-O         Receiver Data Non-Inverted           36         RX4n         CML-O         Receiver Data Inverted           37         GND         Ground           38         RX6p         CML-O         Receiver Data Inverted           40         GND         Ground           41         RX8p         CML-O         Receiver Data Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi-L	24	GND		Ground	
26         RX3p         CML-O         Receiver Data Non-Inverted           27         GND         Ground           28         RX In         CML-O         Receiver Data Inverted           29         RX Ip         CML-O         Receiver Data Non-Inverted           30         GND         Ground           31         GND         Ground           32         RX2p         CML-O         Receiver Data Non-Inverted           34         GND         Ground           35         RX4p         CML-O         Receiver Data Inverted           36         RX4n         CML-O         Receiver Data Inverted           37         GND         Ground           38         RX6p         CML-O         Receiver Data Inverted           40         GND         Ground           41         RX8p         CML-O         Receiver Data Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi-Level         Module Interrupt / Module Reset         2           45         VCC         +3.3V Power           46         VCC         +3.3V Power </td <td>Pin</td> <td>Symbol</td> <td>Logic</td> <td>Description</td> <td>Note</td>	Pin	Symbol	Logic	Description	Note
27         GND         Ground           28         RX In         CML-O         Receiver Data Inverted           29         RX Ip         CML-O         Receiver Data Non-Inverted           30         GND         Ground           31         GND         Ground           32         RX2p         CML-O         Receiver Data Non-Inverted           33         RX2n         CML-O         Receiver Data Inverted           34         GND         Ground           35         RX4p         CML-O         Receiver Data Inverted           36         RX4n         CML-O         Receiver Data Inverted           37         GND         Ground           38         RX6p         CML-O         Receiver Data Inverted           40         GND         Ground           41         RX8p         CML-O         Receiver Data Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi-Level         Module Interrupt / Module Reset         2           45         VCC         +3.3V Power           46         VCC         +3.3V Power	25	RX3n	CML-O	Receiver Data Inverted	
28         RX 1n         CML-O         Receiver Data Inverted           29         RX 1p         CML-O         Receiver Data Non-Inverted           30         GND         Ground           31         GND         Ground           32         RX2p         CML-O         Receiver Data Non-Inverted           33         RX2n         CML-O         Receiver Data Inverted           34         GND         Ground           35         RX4p         CML-O         Receiver Data Inverted           36         RX4n         CML-O         Receiver Data Inverted           37         GND         Ground           38         RX6p         CML-O         Receiver Data Inverted           40         GND         Ground           41         RX8p         CML-O         Receiver Data Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi-Level         Module Interrupt / Module Reset         2           45         VCC         +3.3V Power           46         VCC         +3.3V Power           46         VCC         +3.3V Power<	26	RX3p	CML-O	Receiver Data Non-Inverted	
29         RX 1p         CML-O         Receiver Data Non-Inverted           30         GND         Ground           31         GND         Ground           32         RX2p         CML-O         Receiver Data Non-Inverted           33         RX2n         CML-O         Receiver Data Inverted           34         GND         Ground           35         RX4p         CML-O         Receiver Data Inverted           36         RX4n         CML-O         Receiver Data Inverted           37         GND         Ground           38         RX6p         CML-O         Receiver Data Inverted           40         GND         Ground           41         RX8p         CML-O         Receiver Data Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi-Level         Module Interrupt / Module Reset         2           45         VCC         +3.3V Power           46         VCC         +3.3V Power           47         SDA         LVCMOS-I/O         2-wire Serial Interface Clock         1           48         GND<	27	GND		Ground	
30	28	RX 1n	CML-O	Receiver Data Inverted	
31         GND         Ground           32         RX2p         CML-O         Receiver Data Non-Inverted           33         RX2n         CML-O         Receiver Data Inverted           34         GND         Ground           35         RX4p         CML-O         Receiver Data Non-Inverted           36         RX4n         CML-O         Receiver Data Inverted           37         GND         Ground           38         RX6p         CML-O         Receiver Data Non-Inverted           40         GND         Ground           41         RX8p         CML-O         Receiver Data Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi-Level         Module Interrupt / Module Reset         2           45         VCC         +3.3V Power           46         VCC         +3.3V Power           47         SDA         LVCMOS-I/O         2-wire Serial Interface Clock         1           48         GND         Ground           49         TX7n         CML-I         Transmitted Data Inverted           50 <t< td=""><td>29</td><td>RX 1p</td><td>CML-O</td><td>Receiver Data Non-Inverted</td><td></td></t<>	29	RX 1p	CML-O	Receiver Data Non-Inverted	
32         RX2p         CML-O         Receiver Data Non-Inverted           33         RX2n         CML-O         Receiver Data Inverted           34         GND         Ground           35         RX4p         CML-O         Receiver Data Non-Inverted           36         RX4n         CML-O         Receiver Data Inverted           37         GND         Ground           38         RX6p         CML-O         Receiver Data Non-Inverted           40         GND         Ground           41         RX8p         CML-O         Receiver Data Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi-Level         Module Interrupt / Module Reset         2           45         VCC         +3.3V Power           46         VCC         +3.3V Power           47         SDA         LVCMOS-I/O         2-wire Serial Interface Clock         1           48         GND         Ground           49         TX7n         CML-I         Transmitted Data Inverted           50         TX7p         CML-I         Transmitted Data Non-Inverted	30	GND		Ground	
33         RX2n         CML-O         Receiver Data Inverted           34         GND         Ground           35         RX4p         CML-O         Receiver Data Non-Inverted           36         RX4n         CML-O         Receiver Data Inverted           37         GND         Ground           38         RX6p         CML-O         Receiver Data Non-Inverted           40         GND         Ground           41         RX8p         CML-O         Receiver Data Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi-Level         Module Interrupt / Module Reset         2           45         VCC         +3.3V Power           46         VCC         +3.3V Power           47         SDA         LVCMOS-I/O         2-wire Serial Interface Clock         1           48         GND         Ground           49         TX7n         CML-I         Transmitted Data Inverted           50         TX7p         CML-I         Transmitted Data Non-Inverted           51         GND         Ground	31	GND		Ground	
34         GND         Ground           35         RX4p         CML-O         Receiver Data Non-Inverted           36         RX4n         CML-O         Receiver Data Inverted           37         GND         Ground           38         RX6p         CML-O         Receiver Data Non-Inverted           39         RX6n         CML-O         Receiver Data Inverted           40         GND         Ground           41         RX8p         CML-O         Receiver Data Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi-Level         Module Interrupt / Module Reset         2           45         VCC         +3.3V Power           46         VCC         +3.3V Power           47         SDA         LVCMOS-I/O         2-wire Serial Interface Clock         1           48         GND         Ground           49         TX7n         CML-I         Transmitted Data Inverted           50         TX7p         CML-I         Transmitted Data Non-Inverted           51         GND         Ground	32	RX2p	CML-O	Receiver Data Non-Inverted	
35         RX4p         CML-O         Receiver Data Non-Inverted           36         RX4n         CML-O         Receiver Data Inverted           37         GND         Ground           38         RX6p         CML-O         Receiver Data Non-Inverted           39         RX6n         CML-O         Receiver Data Inverted           40         GND         Ground           41         RX8p         CML-O         Receiver Data Non-Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi-Level         Module Interrupt / Module Reset         2           45         VCC         +3.3V Power           46         VCC         +3.3V Power           47         SDA         LVCMOS-I/O         2-wire Serial Interface Clock         1           48         GND         Ground           49         TX7n         CML-I         Transmitted Data Inverted           50         TX7p         CML-I         Transmitted Data Non-Inverted           51         GND         Ground	33	RX2n	CML-O	Receiver Data Inverted	
36         RX4n         CML-O         Receiver Data Inverted           37         GND         Ground           38         RX6p         CML-O         Receiver Data Non-Inverted           39         RX6n         CML-O         Receiver Data Inverted           40         GND         Ground           41         RX8p         CML-O         Receiver Data Non-Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi-Level         Module Interrupt / Module Reset         2           45         VCC         +3.3V Power           46         VCC         +3.3V Power           47         SDA         LVCMOS-I/O         2-wire Serial Interface Clock         1           48         GND         Ground           49         TX7n         CML-I         Transmitted Data Inverted           50         TX7p         CML-I         Transmitted Data Non-Inverted           51         GND         Ground	34	GND		Ground	
37         GND         Ground           38         RX6p         CML-O         Receiver Data Non-Inverted           39         RX6n         CML-O         Receiver Data Inverted           40         GND         Ground           41         RX8p         CML-O         Receiver Data Non-Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi-Level         Module Interrupt / Module Reset         2           45         VCC         +3.3V Power           46         VCC         +3.3V Power           47         SDA         LVCMOS-I/O         2-wire Serial Interface Clock         1           48         GND         Ground         Ground           49         TX7n         CML-I         Transmitted Data Inverted           50         TX7p         CML-I         Transmitted Data Non-Inverted           51         GND         Ground	35	RX4p	CML-O	Receiver Data Non-Inverted	
38         RX6p         CML-O         Receiver Data Non-Inverted           39         RX6n         CML-O         Receiver Data Inverted           40         GND         Ground           41         RX8p         CML-O         Receiver Data Non-Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi-Level         Module Interrupt / Module Reset         2           45         VCC         +3.3V Power           46         VCC         +3.3V Power           47         SDA         LVCMOS-I/O         2-wire Serial Interface Clock         1           48         GND         Ground         49           49         TX7n         CML-I         Transmitted Data Inverted           50         TX7p         CML-I         Transmitted Data Non-Inverted           51         GND         Ground	36	RX4n	CML-O	Receiver Data Inverted	
39         RX6n         CML-O         Receiver Data Inverted           40         GND         Ground           41         RX8p         CML-O         Receiver Data Non-Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi-Level         Module Interrupt / Module Reset         2           45         VCC         +3.3V Power           46         VCC         +3.3V Power           47         SDA         LVCMOS-I/O         2-wire Serial Interface Clock         1           48         GND         Ground           49         TX7n         CML-I         Transmitted Data Inverted           50         TX7p         CML-I         Transmitted Data Non-Inverted           51         GND         Ground	37	GND		Ground	
40         GND         Ground           41         RX8p         CML-O         Receiver Data Non-Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi-Level         Module Interrupt / Module Reset         2           45         VCC         +3.3V Power           46         VCC         +3.3V Power           47         SDA         LVCMOS-I/O         2-wire Serial Interface Clock         1           48         GND         Ground           49         TX7n         CML-I         Transmitted Data Inverted           50         TX7p         CML-I         Transmitted Data Non-Inverted           51         GND         Ground	38	RX6p	CML-O	Receiver Data Non-Inverted	
41         RX8p         CML-O         Receiver Data Non-Inverted           42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi-Level         Module Interrupt / Module Reset         2           45         VCC         +3.3V Power           46         VCC         +3.3V Power           47         SDA         LVCMOS-I/O         2-wire Serial Interface Clock         1           48         GND         Ground           49         TX7n         CML-I         Transmitted Data Inverted           50         TX7p         CML-I         Transmitted Data Non-Inverted           51         GND         Ground	39	RX6n	CML-O	Receiver Data Inverted	
42         RX8n         CML-O         Receiver Data Inverted           43         GND         Ground           44         INT/RSTn         Multi-Level         Module Interrupt / Module Reset         2           45         VCC         +3.3V Power           46         VCC         +3.3V Power           47         SDA         LVCMOS-I/O         2-wire Serial Interface Clock         1           48         GND         Ground           49         TX7n         CML-I         Transmitted Data Inverted           50         TX7p         CML-I         Transmitted Data Non-Inverted           51         GND         Ground	40	GND		Ground	
43         GND         Ground           44         INT/RSTn         Multi-Level         Module Interrupt / Module Reset         2           45         VCC         +3.3V Power           46         VCC         +3.3V Power           47         SDA         LVCMOS-I/O         2-wire Serial Interface Clock         1           48         GND         Ground           49         TX7n         CML-I         Transmitted Data Inverted           50         TX7p         CML-I         Transmitted Data Non-Inverted           51         GND         Ground	41	RX8p	CML-O	Receiver Data Non-Inverted	
44INT/RSTnMulti-LevelModule Interrupt / Module Reset245VCC+3.3V Power46VCC+3.3V Power47SDALVCMOS-I/O2-wire Serial Interface Clock148GNDGround49TX7nCML-ITransmitted Data Inverted50TX7pCML-ITransmitted Data Non-Inverted51GNDGround	42	RX8n	CML-O	Receiver Data Inverted	
45         VCC         +3.3V Power           46         VCC         +3.3V Power           47         SDA         LVCMOS-I/O         2-wire Serial Interface Clock         1           48         GND         Ground           49         TX7n         CML-I         Transmitted Data Inverted           50         TX7p         CML-I         Transmitted Data Non-Inverted           51         GND         Ground	43	GND		Ground	
46         VCC         +3.3V Power           47         SDA         LVCMOS-I/O         2-wire Serial Interface Clock         1           48         GND         Ground         49         TX7n         CML-I         Transmitted Data Inverted           50         TX7p         CML-I         Transmitted Data Non-Inverted         51         GND         Ground	44	INT/RSTn	Multi-Level	Module Interrupt / Module Reset	2
47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1  48 GND Ground  49 TX7n CML-I Transmitted Data Inverted  50 TX7p CML-I Transmitted Data Non-Inverted  51 GND Ground	45	VCC		+3.3V Power	
48 GND Ground 49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Non-Inverted 51 GND Ground	46	VCC		+3.3V Power	
49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Non-Inverted 51 GND Ground	47	SDA	LVCMOS-I/O	2-wire Serial Interface Clock	1
50 TX7p CML-I Transmitted Data Non-Inverted 51 GND Ground	48	GND		Ground	
51 GND Ground	49	TX7n	CML-I	Transmitted Data Inverted	
	50	TX7p	CML-I	Transmitted Data Non-Inverted	
52 TX5n CML-I Transmitted Data Inverted	51		GND	Ground	
	52	TX5n	CML-I	Transmitted Data Inverted	



53	TX5p	CML-I	Transmitted Data Non-Inverted	
54		GND	Ground	
55	TX3n	CML-I	Transmitted Data Inverted	
56	TX3p	CML-I	Transmitted Data Non-Inverted	
57		GND	Ground	
58	TX 1n	CML-I	Transmitted Data Inverted	
59	TX 1p	CML-I	Transmitted Data Non-Inverted	
60		GND	Ground	

#### **Notes:**

- 1. Open-Drain with pull up resistor on Host.
- 2. See pin description for required circuit.

## VIII. Principle Diagram

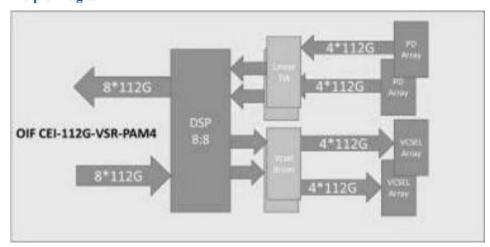


Figure 2. Module Block Diagram

# IX. Digital Diagnostic Monitoring Specifications

Parameter	Specification	Unit
Temperature Monitor Absolute Error	±3	${\mathbb C}$
Supply Voltage Monitor Absolute Error	±5	%
I_Bias Monitor Absolute Error	±10	%
Received Power (Rx) Monitor Absolute Error	±3.0	dB
Transmit Power (Tx) Monitor Absolute Error	±3.0	dB



## X. Mechanical Dimensions

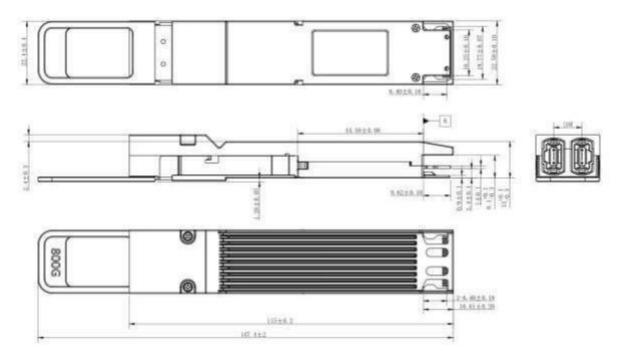


Figure 3. Mechanical Dimensions

## **Order Information**

Part Number	Description
QDD-SR8-800G	800GBASE SR8 QSFP-DD Transceiver, MTP/MPO-16, 50m over MMF
QDD-DR8-800G	800GBASE DR8 QSFP-DD Transceiver, MTP/MPO-16, 500m over SMF
QDD800-XDR8-B1	800GBASEXDR8 QSFP-DD Transceiver, MTP/MPO-16, 2km over SMF
QDD800-PLR8-B1	800GBASE PLR8 QSFP-DD Transceiver, MTP/MPO-16, 10km over SMF
OSFP-SR8-800G	800GBASE SR8 OSFP Transceiver, Dual MTP/MPO-12, 50m over MMF
OSFP-DR8-800G	800GBASE DR8 OSFP Transceiver, MTP/MPO-16, 500m over SMF
OSFP-DR8-800G	800GBASE DR8 OSFP Transceiver, MTP/MPO-12, 500m over SMF
OSFP-2FR4-800G	800GBASE 2FR4 OSFP Transceiver, Dual LC, 2km over SMF
OSFP800-XDR8-B2	800GBASEXDR8 OSFP Transceiver, MTP/MPO-12, 2km over SMF
OSFP800-XDR8-B1	800GBASEXDR8 OSFP Transceiver, MTP/MPO-16, 2km over SMF
OSFP800-2LR4-A2	800GBASE 2LR4 OSFP Transceiver, Dual LC, 10km over SMF
OSFP800-PLR8-B1	800GBASE PLR8 OSFP Transceiver, MTP/MPO-16, 10km over SMF
OSFP800-PLR8-B2	800GBASE PLR8 OSFP Transceiver, MTP/MPO-12, 10km over SMF